

Attachment A

Version of Claim showing changes made

The deletion is shown in brackets.

52. The memory circuit of claim 51 [a] further comprising:

an address bus for receiving a burst address; and

a control input terminal for receiving a read/write control signal for indicating a read burst or a write burst operation,

wherein the first read burst operation is initiated upon a rising edge of a clock cycle by asserting the read/write control signal to indicate a read burst operation and providing a first burst address at the address bus both prior to the rising edge of the clock cycle, the first and second data items representing a burst of two data items corresponding to the first burst address.